IV. REMARKS

Claims 1-11 are pending in this application. Applicants do not acquiesce in the correctness of the objections and rejections and reserve the right to present specific arguments regarding any rejected claims not specifically addressed. Further, Applicants reserve the right to pursue the full scope of the subject matter of the original claims in a subsequent patent application that claims priority to the instant application. Reconsideration in view of the above amendments and following remarks is respectfully requested.

Entry of this Amendment is proper under 37 C.F.R. §1.116(b) because the Amendment: (a) places the application in condition for allowance as discussed below; (b) does not raise any new issues requiring further search and/or consideration; and (c) places the application in better form for appeal. Accordingly, Applicants respectfully request entry of this Amendment.

Applicants note that the pending claims are incorrectly cited on the Office Action summary as 1-10, rather than 1-11. Correction is requested.

With regard to the Office's statement regarding the improper listing of references, Applicants believe that Information Disclosure Statements (IDS) for all references listed were submitted. In particular, an IDS for non-patent references was submitted on 12/16/02 and initialed by the Office. In addition, an electronic IDS for US patents was submitted with the application. Clarification as to which references have not been properly cited is respectfully requested.

In the Office Action, the specification was objected to because of informalities. By this amendment, the specification has been amended to correct the typographical error. Accordingly, Applicants request withdrawal of the rejection.

In the Office Action, claim 6 was rejected under 35 U.S.C. §102(b) as being anticipated by Yamaguchi *et al.*, *Process and Device Optimization of an Analog Complementary Bipolar IC Technology With 5.5-GHz fT PNP Transistors*, hereinafter "Yamaguchi *et al.*;" claims 1-3, 5, 7 and 9 were rejected under 35 U. S. C. 103(a) over Yamaguchi *et al.* and Babcock *et al.* (U.S. Publication No. 2003/0080394), hereinafter "Babcock *et al.*;" claim 4 was rejected under 35 U. S. C. 103(a) over Yamaguchi *et al.* in view of Babcock *et al.* and Goth (U.S. Patent No. 4,719,185), hereinafter "Goth;" and claim 8 was rejected under 35 U. S. C. 103(a) over Yamaguchi *et al.*; claim 10 was rejected under 35 U.S.C. 103(a) over Yamaguchi *et al.*, in view of Babcock *et al.* and Harame *et al.* (U.S. Patent No. 4,997,776), hereinafter "Harame *et al.*;" and claim 11 was rejected under 35 U.S.C. 103(a) over Yamaguchi *et al.* in view of Goth. Applicants submit that the pending claims are allowable and thus respectfully request withdrawal of the rejections.

With respect to claim 6, Yamaguchi *et al.* fail to disclose each and every claimed feature. The present invention recites, *inter alia*, "a single layer of silicon that forms an emitter region of the PNP transistor, an extrinsic base region of the NPN transistor and an intrinsic base region of the NPN transistor." First, Applicants submit that Yamaguchi *et al.* only mention P^+ (or N^+) implants for PNP collector contact and NPN extrinsic base region and there is no mention of a single layer that forms emitter region of PNP transistors and extrinsic and intrinsic base region of NPN transistors.

Second, although Yamaguchi *et al.* mention sharing collector contact implants for the PNP transistors with a P^+ extrinsic base implant for the NPN transistors (Yamaguchi *et al.* at 1023 –24; Fig. 1), they do not disclose the same regarding the emitter region of the PNP

transistor. In Yamaguchi *et al*, the PNP collector contact is specifically distinguished with the PNP emitter region. (*See* Fig. 1, the collector being marked as "c" and the emitter being marked as "e"). In contrast, the present invention discloses, *inter alia*, "a single layer of silicon that forms an emitter region of the PNP transistor, an extrinsic base region of the NPN transistor[.]"

Third, Yamaguchi *et al.* do not disclose sharing collector contact implants for PNP transistors with a P^+ intrinsic base implant for NPN transistors. In Yamaguchi *et al.*, the NPN extrinsic base implant masks and the intrinsic base implant masks are listed together, but only the elimination of the PNP extrinsic base implant masks is specifically disclosed, which indicates that Yamaguchi *et a*l. do not anticipate the elimination of NPN intrinsic base implant masks. In other words, Yamaguchi *et al.* do not anticipate sharing the intrinsic base regions implants for the NPN transistors with the collector contact implants for the PNP transistors. *See* Yamaguchi *et al.* at 1020. So even if the implants of P^+ are taken as equal to a "layer," in Yamaguchi *et al.*, the collector contact of the PNP is not formed on the same layer as the intrinsic base region of the NPN transistor because they are not formed by the same implant of P^+. In view of the foregoing, Yamaguchi *et al.* do not disclose "a single layer of silicon that forms an emitter region of the PNP transistor, ... and an intrinsic base region of the NPN transistor[,]" as recited in claim 6. Accordingly, claim 6 of the present invention is not anticipated by Yamaguchi *et al.* Applicants respectfully request withdrawal of the rejections.

With respect to claim 1, Applicants submit that there is no suggestion or motivation to combine Yamaguichi *et al.* and Babcock *et al.* In Babcock *et al.*, carbon or other cabon-bearing species such as SiGeC is used to retard the diffusion of the common P-type dopant, e.g., boron, and common n-type dopant. Note Page 3, Paragraph 0034. Retarding diffusion of P-type dopant

is not a concern in Yamaguchi *et al.* Therefore, it is incomprehensible why a person having ordinary skill in the art would modify Yamaguchi *et al.* to incorporate Babcock *et al.*

In addition, even if Yamaguchi *et al.* and Babcock *et al.* are combined, the combination does not disclose or suggest each and every claimed feature of claim 1. Similar to the analysis regarding claim 6, Yamaguchi *et al.* do not disclose or suggest, *inter alia*, "an intrinsic base region of the vertical NPN transistor located in the same layer as the emitter region of the vertical PNP transistor[,]" as recited in claim 1. Babcock *et al.* do not overcome this deficiency of Yamaguchi *et al.* Moreover, Babcock *et al.* do not disclose or suggest the claimed invention including "an emitter region of the vertical PNP transistor including silicon and germanium[,]" as recited in claim 1. What Babcock *et al.* disclose is "carbon-bearing species such as SiGeC" included in emitter polysilicon layer (35) to retard diffusion of p-type dopant from the emitter polysilicon layer (35) to the active emitter region (40). *See* Abstract and Paragraph 42. In Babcock *et al.*, there is no disclosure or suggestion of germanium in the active emitter region (40). Therefore, Babcock *et al.* do not disclose or suggest "an emitter region of the vertical PNP transistor including silicon and germanium." Yamaguchi *et al.* do not overcome this deficiency of Babcock *et al.* Accordingly, Applicants respectfully request withdrawal of the rejections.

Claims 2-5 are dependent upon claim 1 and claims 7-11 are dependent upon claim 6. Applicants submit that those dependent claims are allowable for the same reasons stated above, as well as for their own additional features.

Applicants respectfully submit that the application is in condition for allowance. Should the Examiner believe that anything further is necessary to place the application in better condition for allowance, he is requested to contact Applicant's undersigned attorney at the telephone number listed below.

Respectfully submitted,

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